Advanced Packaging

Cost Benefit of Strip Test

STRIP TEST REDUCES COST OF FINAL MANUFACTURING.

BY DAVE HUNTLEY

A major challenge facing the semiconductor manufacturing industry is increasing the efficiency of final manufacturing processes. The migration of cost structure from wafer fab toward final manufacturing has placed it in the crosshairs of fiscal scrutiny and revealed economic and technical issues that could conceivably impair some manufacturers' economic viability.

The overall cost of final manufacturing (test, assembly and packaging) is a crucial area that manufacturers will have to address as they move forward. With packaging costs relatively flat and average selling price erosion running at 15-20 percent per year, final manufacturing will likely account for as much as 80 percent of product cost within 15 years. Today, final manufacturing can make up 50 percent of the product cost, and yet capital investment is dwarfed by that invested in wafer fab. This imbalance in product cost vs. investment will have to be corrected if the industry is to stay on track with Moore's law. Strip test vs. singulated test is one area that increased investment in final manufacturing may provide a significant payoff.

The Cost of Test

The cost of test is a significant portion, approximately 33 percent, of final manufacturing costs. Current test strategies contain some glaring inefficiencies. Reducing the cost of test offers promising opportunities to reduce the cost of final manufacturing.

Tester cost is rising, as they become increasingly sophisticated to match the demands placed upon them by the ever more complex devices they must test. While initiatives to include built-in self-test (BIST) on the device itself may alleviate the problem and slow the increase in tester cost, the overall upward direction is unlikely to change. The only option to reduce the cost of test is to increase the use of the tester.

The most common test strategy today is to do simple test at wafer probe to screen out nonfunctional devices, and then perform burn-in and full-functional testing of the packaged and singulated device as the last step before shipping the product. Unfortunately, there are a number of inefficiencies in this approach.

Parallel test. Testers used in wafer probe are capable of testing as many as 128 devices in parallel. Such parallelism would significantly reduce the test time per device in final test, but is prevented by today's handler constraints. In some cases, a number of devices are first loaded into an alignment carrier and tested in parallel. This reduces the handling time per device and reduces the probability of handling jams while the tester waits. However, loading the alignment carrier is an additional step and requires a complex change kit for each product type.

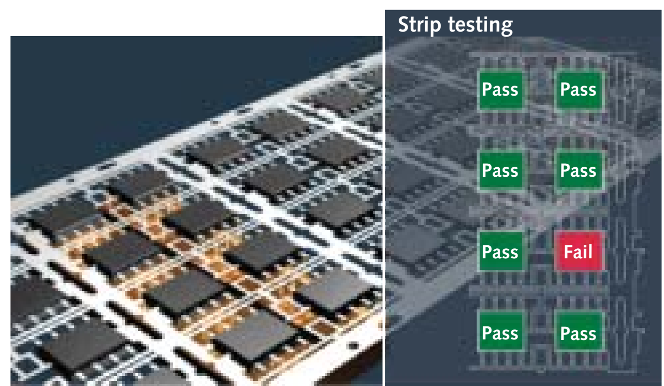

Figure 1. Strip testing in action

Handling time and reliability. The tester is idle as each singulated device is loaded into the test position. A singulated device is difficult to handle, so handling time is significant and the possibility of jams is comparatively high. This is especially true for small devices.

Alignment accuracy. For devices with fine contact pitch, alignment to the probe contacts must be extremely precise. Alignment to very fine pitch contacts is possible at wafer probe since the devices are an integral part of the precisely manufactured wafer. It is much harder to guarantee alignment accuracy for a singulated device placed in an alignment pocket. The result is yield loss, caused by contact misses.

The right tester for the job. Final test now includes advanced parametric testing, as well as the simpler functional testing. For some portion of the test cycle an advanced (and expensive) tester is performing a simple test task.

If we can reduce the handling time per device, improve the alignment accuracy, test as many devices in parallel as the tester will allow, and separate advanced and simple tests so that opti-

Reprinted with revisions to format, from the November 2003 edition of **ADVANCED PACKAGING**
Copyright 2003 by PennWell Corporation

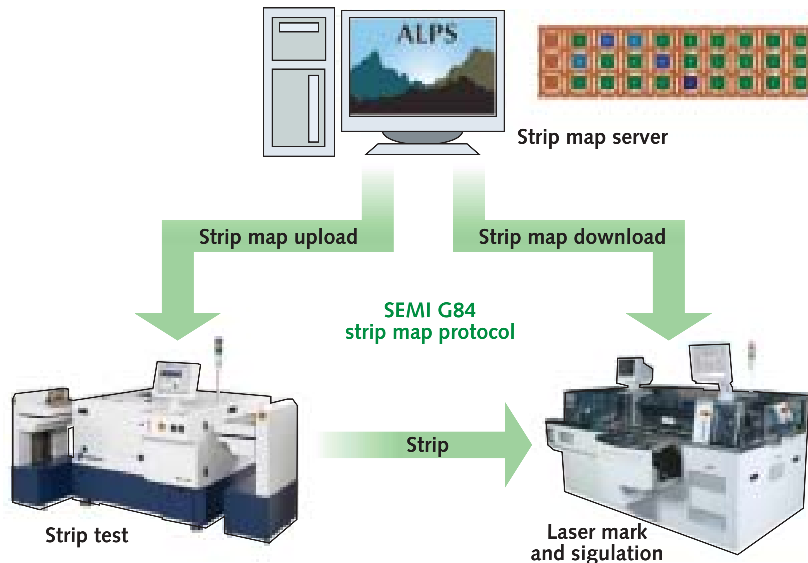

Figure 2. Handling strip maps

mized cost-effective testers can be used for each test, then the cost of test in final manufacturing will be substantially reduced.

Strip Test

The term "strip test" refers to testing the devices in strip (ie., leadframe, solid BGA strip, etc.) form. Before testing, the devices must be electrically isolated and yet remain physically attached to the strip. The strip is then loaded into a strip test handler where it is indexed to align with an array of probe contacts connected to the tester. The device array is contacted and tested, and then the strip is indexed to the next device array and so on.

One strip test drawback is the additional electrical isolation process step compared to singulated test. The cost and reliability of this additional step must be factored into any cost-benefit analysis. Another drawback is the higher capital cost of the strip handler. It is all well and good to argue, as we do in this article, that the investment will pay for itself. However, the initial cost may prove too daunting for some — especially during the extended downturn we have endured. Fortunately, the cost of strip handlers is now responding to competitive pressure. As more players enter the market, capital cost becomes less of an issue. Despite these drawbacks, strip test promises to address many of the inefficiencies of current test strategies.

Benefits

Since the devices are already in a matrix form on the strip, they can be tested in parallel without requiring an additional step to assemble the matrix. Furthermore, a strip often contains sufficient devices to make full use of the parallel test capabilities of the tester.

Strips are larger and more uniform than singulated devices, and much easier to handle. The overhead time for handling a strip is similar to handling a singulated device, and the probability of jams is much lower. Handling overhead per device can be reduced approximately in proportion to the number of devices on the strip, thereby keeping tester idle time to an absolute minimum.

Like a wafer, a strip contains devices that are precisely aligned on the substrate. It is therefore possible to reliably make contact with finer pitch contacts on the device when in strip form than can be achieved when the devices have been singulated. The expertise from the field of wafer probe is now being applied to the challenges of contacting these fine pitch contacts.

Wafers are normally probed to screen out failures at the wafer level, and then the devices are subjected to final test once packaged. Between 3-10 percent of the devices that pass wafer probe screening subsequently fail final test. This is bad enough for individual devices, but when devices are stacked the yield loss of each device is multiplied. To avoid this, full burn-in and functional test should be performed at the wafer level to ensure that only known good die are assembled into the stack.

An argument can be made for performing full-functional testing upstream at the wafer level, even for single device packages, so that devices that fail final test do not use up an expensive package. If the more complete and advanced tests are performed at the wafer level with the expensive test equipment, then all that is needed at strip test is weeding out package-induced errors. Such testing is quicker and requires less costly test equipment.

Strip test addresses all of the major inefficiencies in today's test strategies using singulated test. Strip test offers the most cost savings for small devices, along with short test times. Apart from microprocessors, most of the devices in volume production are small. As the trend to move full-functional testing upstream to the wafer level increases, the test time at strip test will decrease. Actual cost savings will be dependent on test time, device size and contact pitch, but they are already compelling and heading in the right direction.

Strip Mapping

Early strip test lines had a laser marker integrated physically inline with the strip handler. The strip map containing bin codes for sorting was fed forward directly to the laser marker so that bad devices could be marked or left unmarked, while good devices receive a full device mark that is used to sort out good devices after singulation. This is analogous to using ink dots to mark bad devices at wafer probe. An advantage of this rigid inline integration is that strip maps are passed to the laser mark in the same order as the strips themselves, so it can be assumed that the next strip map always relates to the next strip. This prevents the need to mark the strip with a matrix identifier.

Rigid in-line integration does, however, prevent line balancing. Depending upon the device characteristics, the strip test or the laser mark step will be the bottleneck to throughput. Decoupling the laser mark from strip test allows more flexibility in balancing the line, but strips do need to have a matrix identifier mark because the sequence of strips at strip test will

not necessarily match the sequence of strips that arrives at each laser marker.

After strip test, the strip map will be uploaded with the strip identifier to be stored in a strip map database. The laser marker then requests the map, based on the strip identifier. This is analogous to how wafer maps are managed from wafer probe to die attach.

Once strip maps are identified and a map server is in place, it becomes possible to sort devices based on the map rather than depend on the laser mark. For strip maps to be shared across equipment in this manner, there must be an interface between the equipment and the strip mapping system. Semiconductor Equipment and Supplies International has taken the initiative to develop standards for substrate mapping (SEMI G81, G84 and G85) that incorporate both wafer and strip maps.

Status and Outlook

In 2001, Amkor, a provider of semiconductor assembly and test services, invested $50 million to develop strip testing. Last year they reported test cost savings of as much as 80 percent. A handful of other strip test lines are now in operation, but the overall adoption of strip test has been sluggish. The blame may be fairly attributed to the long, deep recession the industry has just endured. It would take a brave manager to commit to the high capital cost of converting to strip test while the cost-reduction benefits were still unproven.

Today, however, we are emerging from the recession and there is hard data to support the cost savings associated with strip test. Cost savings achieved vary depending on the device and package type, but values of 20 percent are not uncommon. Equipment suppliers are joining the market for strip handlers, and competition will apply downward pressure on prices. This should lower initial capital costs.

MCT was the first prominent supplier of strip handlers, but Delta Design and ASM are not far behind. At Semicon West this year, several more companies — including Electroglas and Microtest — announced strip test solutions. Laser mark and singulation equipment vendors have also recognized the opportunity and are offering strip-map-enabled versions of their equipment for integration into the strip test line. Clearly, these companies see the potential for significant growth in the strip test market.

Conclusion

Strip test offers an opportunity to significantly reduce the cost of test in final manufacturing. Although adoption has been slow so far, strip test is now poised for growth as more companies introduce products to address the market. Strip test will be one of the technologies that will allow final manufacturing to fulfill the promise of Moore's law. **AP**

DAVE HUNTLEY, president, may be contacted at Kinesys Software Inc., 6 C St., Petaluma, CA 94952; (707) 766-8196; e-mail: dave.huntley@kinesysinc.com.